RESPONSE/REMARKS

The present Response is in response to the Final Office Action having a mailing date of January 22, 2004. Claims 1-9 are pending in the present Application.

In the above-identified Office Action, the Examiner rejected claims 1-9 under 35 U.S.C. § 103 as being unpatentable over Japanese Patent JP411204854A (Mizushima). In response to Applicant's previous arguments, the Examiner stated:

> **In fig. 10, Mizushima shows another variation of the same inventive concept in which the "gate resistor" is replaced by transistor 9 for even more stabilized operation from the identical concept and the MTJ is nevertheless labeled 4 (here, 4 is drawn identically to 1 in fig. 1).**
>
> **From another view point, it is inherent in magnetic memory specifications that in fig. 10, 4 has to be a MTJ because if 4 was not, there is no other place in the drawing of the memory cell of fig 10 [that] would an MTJ be [sic] and that simply does not make sense for magnetic memory cell [to be] without an MTJ, or TMR (tunneling magneto resistor), which is essential for storing data.**

Applicant respectfully disagrees with the Examiner's rejection. Independent claim 1 recites

> [a] magnetic memory cell comprising:
>
> a magnetic tunneling junction including a first ferromagnetic layer, a second ferromagnetic layer and an insulating layer between the first ferromagnetic layer and the second ferromagnetic layer; and
>
> a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell.

Similarly, independent claim 5 recites:

> [a] magnetic memory comprising:
>
> a plurality of memory cells arranged in an array including a plurality of rows and a plurality of columns, each of the plurality of memory cells including a magnetic tunneling junction and a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end of the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell;

a plurality of row lines coupled to the plurality of rows, the plurality of row lines coupled to gate of the transistor in each of the plurality of memory cells in the plurality of rows;

a row selector coupled to the plurality of row lines for selecting between the plurality of row lines and providing a current to a selected row of the plurality of rows.

Thus, the magnetic memory cells of claim 1 and claim 5 include a magnetic tunneling junction having a first end coupled to the gate of a transistor and a second end coupled to the source of the transistor. Claims 1 and 5 also recite that the output is coupled to the drain of the transistor. Because of the configuration of the magnetic tunneling junction, the transistor, and the output, the magnitude of the signal, as well as the difference in signal between different states of the magnetic tunneling junction, are significantly larger. Specification, page 7, lines 16-24.

The cited portions of Mizushima fail to teach or suggest the recited magnetic tunneling junction coupled to the gate and source of the transistor in combination with the drain of the transistor being coupled to the output. In particular, Mizushima does not couple the source of the transistor with a second end of the magnetic tunneling junction and connect the drain of the transistor with the output.

As discussed previously, Fig. 1 of Mizushima discloses a cell which includes a magnetic tunneling junction device 1, a transistor 2 and a gate resistor 4. Abstract, Mizushima. As can be seen in Fig. 1, the cell of Mizushima does not have the gate and source of the transistor 2 coupled with opposing ends of the magnetic tunneling junction 1 in combination with the drain of the transistor 2 connected to the output. Fig. 1 of Mizushima thus fails to teach or suggest the recited cell and memory of claims 1 and 5, respectively.

Fig. 10 of Mizushima also fails to teach or suggest the recited combination of the magnetic tunneling junction and transistor. As the Examiner has acknowledged, the cell depicted in Fig. 10

of Mizushima includes an additional transistor 9. However, in contrast to the Examiner's conclusion, the transistor 9 does not replace the gate resistor and the gate resistor 4 does not become the magnetic tunneling junction device. Instead, the transistor 9 replaces the magnetic tunneling junction 1, while the gate resistor remains essentially unchanged.

The transistor 9 is a hot electron transistor that is used as a GMR element. See Japanese Patent Office translation, paragraph 82-83 of operation (http:/www4.ipdl.jpo.go.jp/cgi-bin/tran_web_cgi_ejje). Consequently, the transistor 9 stores data. Furthermore, Mizushima states that no additional discussion is provided for elements in Fig. 10 that correspond to elements of Fig. 1. Japanese Patent Office translation, paragraph 82 of operation. Applicant has found no mention in the translation of the element 4 changing from a gate resistor to a magnetic tunneling junction device. Therefore, the resistor 4 of Fig. 10 remains a (variable) gate resistor and the transistor 9 is used to store data.

The cell depicted in Fig. 10, therefore, contains a GMR transistor 9 in lieu of a magnetic tunneling junction 1, but still utilizes a gate resistor 4. Thus, although the cell depicted in Fig. 10 of Mizushima stores data, the cell does not include a magnetic tunneling junction. The connections to the storage portion (the transistor 9), gate resistor 4, and transistor 2 also remain analogous to those in Fig. 1. Because Fig. 10 omits a magnetic tunneling junction and because the connections between the data storage portion and transistor of Fig. 10 of Mizushima are analogous to Fig. 1 of Mizushima, Fig. 10 of Mizushima still fails to teach or suggest the recited magnetic tunneling junction coupled to the gate and source of the transistor in combination with the drain of the transistor being coupled to the output. Consequently, the cited portions of Mizushima fail to teach or suggest the magnetic memory cell and magnetic memory recited in claims 1 and 5, respectively.

Accordingly, Applicant respectfully submits that claims 1 and 5 are allowable over the cited references.

Claims 2-4 and 6-9 depend upon claims 1 and 5, respectively. Consequently, the arguments herein apply with full force to claims 2-4 and 6-9. Accordingly, Applicant respectfully submits that claims 2-4 and 6-9 are allowable over the cited references.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

SAWYER LAW GROUP LLP

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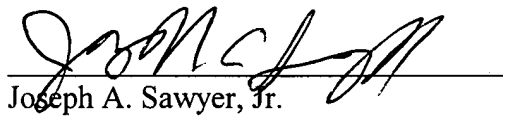

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